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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,859	06/26/2006	Michael H. McKerreghan	102416-108	4650

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WIGGIN AND DANA LLP
ATTENTION: PATENT DOCKETING
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EXAMINER	
HA, NATHAN W	
ART UNIT	**PAPER NUMBER**
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09/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,859	MCKERREGHAN ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo (US 6,858,919, previously cited) and in view of Minamio et al. (US 6,680,524, previously cited, and hereinafter, Miamio.)

3. In regard to claim 1, Seo discloses an integrated circuit device package (103) in fig. 4b, comprising: an integrated circuit device (2) having an electrically active surface (2b) and an opposing backside surface (2c) and sides (vertical side) extending therebetween, said electrically active surface (2b) having a plurality of electrically active circuit traces formed thereon and metallized bumps (2a) extending from selected sites on said circuit traces; a plurality of electrically conductive leads (6) each having respective first surfaces and opposing second surfaces; a plurality of electrical contacts (12) extending outward from said respective first surfaces; a solder (8) electrically and mechanically bonding said metallized bumps (2a) to said second surfaces; and a dielectric molding resin (10) formed into a package at least partially encapsulating said integrated circuit device (2) and said plurality of electrically conductive leads (6),

said backside surface (2c) and said plurality of electrical contacts (12) are exposed on opposing sides of said package.

Seo, however, does not expressly disclose that the back side area to be less than the active surface area in order to provide a locking feature which happens inherently by the shape of the device. Nevertheless, it should be noted that the locking feature as claimed is widely used in semiconductor packages since such feature would allow the chip to be centralized inside the encapsulant material preventing any damage might happen during shipping or normal operation of the chip.

For instance, Minamio, in front figure, discloses an analogous semiconductor package including all of the limitations and further teaches that the back side surface area of the chip 9 is less than the active surface area in order to provide better secure between the resin and the chip, and so the resin and the wiring substrate. See the abstract. Minamio further discloses that the back has an interface which has an end portion between the chip and the molding.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide a locking portion as taught by Minamio in Seo in order to take the advantage as mentioned.

In regard to claim 4, Seo discloses the package (103) of claim 2 wherein a thickness of said package is less than three times a thickness of said integrated circuit device (the molding is coplanar to the surface of the IC), fig. 4b.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seo and Minamio and in view of US 6759745 to Masumoto et al (previously cited, and hereinafter, Masumoto.)

In regard to claim 3, the combination of Seo and Minamio does not disclose the package (103) wherein said at least one feature includes two elements that intersect at an angle of approximately 90°.

However, Masumoto discloses a package in fig. 5 comprising a die (500) having at least one feature includes two elements (step portion at 517) that intersect at an angle of approximately 90°. At the time the invention was made; it would have been obvious to a person having ordinary skill in the art to incorporate the die having step portion teaching of Masumoto in the package of Seo, because it would have reduced the amount of the fillet spread out around semiconductor chip as taught by Masumoto, see abstract.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Seo and Minamio and in view of US 6700206 to Kinsman et al (previously cited.)

In regard to claim 5, the above combination fails to disclose the package of claim 4 wherein said thickness of said package is approximately 0.01 inch.

However, Kinsman discloses a package (10), in fig. 1B, having a thickness approximately 0.012 inch, col. 6 line 20. Accordingly, it would have been obvious to one of ordinary skill in art to use the thickness teaching of Kinsman in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum

or workable range by routine experimentation, MPEP 2144.05, and such package thickness is typical in the art.

6. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seo and Minamio and in view of US 7192789 to Okada et al. (previously cited.)

In regard to claims 6-7, the above combination fails to disclose the package wherein said integrated circuit device is a sensor responsive to external stimulus, wherein said external stimulus is a touch. However, Okada discloses a package in fig. 5 or 7comprising an IC (2) having an exposed surface wherein said IC (2) is a sensor responsive to external stimulus, wherein said external stimulus is a touch (finger sensor). At the time the invention was made; it would have been obvious to a person having ordinary skill in the art to use the finger sensor teaching of Okada in the package of Seo/Minamio for an intended purpose such as touch sensitive device.

Response to Arguments

7. Applicant's arguments filed 9/9/08 have been fully considered but they are not persuasive. Applicants argue that the combination does not disclose the current claimed invention such the chip has an interface as recited in claim 1. First, Minamio discloses this feature in figures 3, 7B, 9A and 9B. It is commonly used in the art of packaging to use this feature as a locking device in a resin compound. The Minamio is incorporated therein to simply show the obviousness of such feature. Applicants further argue that the feature as taught by Minamio is just a straight line, not an interface as currently claimed. Figure 3 of Minamio is a cross section of the whole package. The L-shape

feature is a combination of plane 10a and the vertical plane. These planes are considered to be interface planes. Plane 10a is parallel to the back surface 10B, or face, of the chip. This feature is identical with the feature as currently claimed. It is not understood how this feature can be different from the feature as mentioned by the applicants in fig. 2. The combination shows the back side of the chip is exposed. See also Minamio's col. 7, lines 13-23.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nathan W. Ha/
Primary Examiner, Art Unit 2814